PERSONAL INFORMATION

Oana Amaricai-Boncalo

Date of birth ' | Nationality

WORK EXPERIENCE

Feb 2017 – Present
Associate Professor
University Politehnica Timisoara
Department of Computer and Information Technology

Sept 2012 – Feb 2017
Lecturer
University Politehnica Timisoara
Department of Computer and Information Technology

Feb 2009 – Sept 2012
Teaching Assistant
University Politehnica Timisoara
Department of Computer and Information Technology

EDUCATION AND TRAINING

2019
Habilitation - Thesis Title: Layered LDPC Decoding Architectures:bridging the Gap from Algorithms to Implementations
University Politehnica Timisoara

2006-2009
PhD - Thesis Title: "Simulation Based Reliability Analysis of Quantum Circuits"
University Politehnica Timisoara

2001–2006
Engineering Degree in Computer Engineering
University Politehnica Timisoara
Faculty of Automation and Computers

PERSONAL SKILLS

Mother tongue   Romanian

Other languages

UNDERSTANDING		SPEAKING		WRITING
Listening	Reading	Spoken interaction	Spoken production	
English				
C1	C2	C1	C1	C2
French				
A2	A1	A1	A2	A2

Levels: A1 and A2: Basic user – B1 and B2: Independent user – C1 and C2: Proficient user
Common European Framework of Reference for Languages

RESEARCH ACTIVITY

Research projects
- Principal investigator for 3 research projects (2 international and 1 national), and member in the implementation team for 5 project
- Consortium manager for European Space Agency project REDOUBT - Reliable FPGA Datapath Design Using Control Feedback Loops
- Principal Investigator for Romanian partner in bilateral French-Romanian ANR-UEFISCDI project DIAMOND - French project partners: CEA-LETI Grenoble (dr. Valentin Savin) and ETIS Cergy-Pontoise (Prof. David Declercq)

Research visits
- June-July 2012 - University College Cork, Ireland
- Jan-Feb 2016 - University of Cergy-Pontoise, France

Reviewer
- Sep 2017 – present - Handling editor for Microprocessors and Microsystems - Embedded Hardware Design
- Reviewer activity for : IEEE Trans. on Circuits and Systems, IEEE Trans. on VLSI, IEEE Access, Integration - the VLSI Journal
- Program Committee member for: Euromicro Digital System Design (2018-present), IEEE CIT (2008-2011), TrustComm (2012, 2014), IEEE iNIS (2016)

Publications
- 67 peer-reviewed papers, of which 15 ISI rated journals
- Co-inventor for "Stopping criterion for decoding Quasi-Cyclic LDPC codes" USPO US10651872B2, and EPO EP3373488B1
- Most relevant 5 papers:
  - O Boncalo, G Kolumban-Antal, A Amaricai, V Savin, D Declercq "Layered LDPC Decoders With Efficient Memory Access Scheduling and Mapping and Built-In Support for Pipeline Hazards Mitigation" IEEE Transactions on Circuits and Systems I: Regular Papers 66 (4), 2019 (IF 3.318, Q1)
  - K Le, D Declercq, F Ghaffari, L Kessal, O Boncalo, V Savin "Variable-node-shift based architecture for probabilistic gradient descent bit flipping on QC-LDPC codes" IEEE Transactions on Circuits and Systems I: Regular Papers 65 (7),2018 (IF 3.318, Q1)
  - TT Nguyen-Ly, V Savin, K Le, D Declercq, F Ghaffari, O Boncalo "Analysis and design of cost-effective, high-throughput LDPC decoders" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 26 (3), 2018 (IF 2.037 Q2)
  - D Declercq, V Savin, O Boncalo, F Ghaffari "An imprecise stopping criterion based on in-between layers partial syndromes" IEEE Communications Letters 22 (1), 2018 (IF 3.419, Q2)
  - O. Boncalo, A. Alexandru, Z. Lendek "Fault Tolerant Digital Data-Path Design via Control Feedback Loops" Electronics, 2020 (IF 2.412 , Q2)