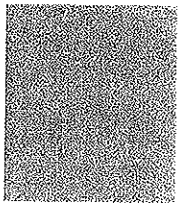
PERSONAL INFORMATION

Alexandru Amăricăi-Boncalo



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Sex Male | Date of birth 15/12/1982 |

WORK EXPERIENCE

2016 – present — Associate Professor
University Politehnica Timisoara
- Teaching and Research Activities

2009 – 2016 — Assistant Professor
University Politehnica Timisoara
- Teaching and Research Activities

2006 – 2009 — PhD candidate
University Politehnica Timisoara
- Teaching and Research Activities
- Thesis title: On the Design of Floating Point Units for Interval Arithmetic
- PhD. Advisor: Prof. Mircea Vladutiu

EDUCATION AND TRAINING

2001 - 2006 — University Politehnica Timisoara
Faculty of Automatics and Computers
- Computer and Software Engineering

PERSONAL SKILLS

Mother tongue(s): Romanian/Serbian

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1

Levels: A1/A2: Basic user - B1/B2: Independent user - C1/C2 Proficient user
Common European Framework of Reference for Languages

ADDITIONAL INFORMATION

Projects
Principal Investigator

- 2007 – 2008, "On the Design of Floating Point Units for Interval Arithmetic", Research Project for Young PhDs, PN-II-RU-TD-26/2007, funded by the UEFISCDI
- 2011 – 2014, "FLAG - FLoating point Arithmetic units for Graphical applications in FPGAs", Research Project for Young Researcher Teams, PN-II-RU-TE-2011-3-0186, funded by the Romanian Ministry of Education and Research.
- 2013 – 2016, FP7-FET Open" i-Risc Innovative Reliable Chip Design from Low Power Unreliable Components", Consortium: CEA-LETI Grenoble (Coordinator), ENSEA, Cergy-Pontoise, TU Delft, UP Timisoara, University College Cork, ELFAK Nis (Serbia);
- 2015-2017 CHIST-ERA"DIVIDEND Distributed Heterogeneous Vertically IntegrateD ENergy Efficient Data centres" ; Consortium: Univ. of Edinburgh (Coordinator), Univ. of Lancaster, Queens University of Belfast, EPF Laussane, UP Timisoara, INRIA Paris, AMD Paris;

Primary technical interests

1. RTL Design of DSP IP Cores
2. Experience with Error Correction Codes (in particular LDPC), as well as Floating Point Arithmetic

Technical skills

1. RTL design: Verilog/VHDL – experience with Xilinx ISE/Vivado
2. Front-end verification: SystemVerilog – experience with Modelsim
3. Software development: C/C++
4. Matlab (beginner level)

Relevant Publications

1. O. Boncalo, A. Amaricai "Ultra High Throughput Unrolled Layered Architecture for QC-LDPC Decoders" IEEE Symposium on VLSI, 2017
2. O. Boncalo, A. Amaricai, P.F. Mihancea, V. Savin ," Memory Trade-offs in Layered Self-Corrected Min-Sum LDPC Decoders" Analog Integrated Circuits and Signal Processing, Vol. 87, Issue 2, 2016
3. Oana Boncalo, Petru Florin Mihancea, Alexandru Amaricai "Template-based QC-LDPC decoder architecture generation" Proc. 10th International Conference on Information, Communications and Signal Processing (ICICS), 2015
4. A.Amaricai, V. Savin, O. Boncalo, N. Cucu-Laurenciu, J. Chen, S. Cotofana , "Timing error analysis of flooded LDPC decoders" Proc. 2015 Conference on Microwaves, Communication, Antennas and Electronic Systems (COMCAS), 2015
5. Alexandru Amaricai, Nicoleta Cucu-Laurenciu, Oana Boncalo, Joyan Chen, Sergiu Nimara, Valentin Savin, Sorin Cotofana "Multi-level probabilistic timing error reliability analysis using a circuit dependent fault map generation", Proc. 2015 Conf. on Design of Circuits and Integrated Systems (DCIS), 2015
6. O. Boncalo, A. Amaricai, V. Savin, D. Declercq, F. Ghaffari "Check node unit for LDPC decoders based on one-hot data representation of messages" IET Electronics Letters, Vol. 51, Issue 12, 2015
7. O. Boncalo, A. Amaricai, C. Spagnol, E. Popovici "Cost effective FPGA probabilistic fault emulation" Proc. Nordic Microelectronics Event NORCHIP, 2014
8. A.Amaricai, C.E. Gavriliu, O. Boncalo ," An FPGA sliding window-based architecture harris corner detector" Proc. 24th Int. Conf. on Field Programmable Logic and Applications (FPL),2014
9. A.Amaricai, C.E. Gavriliu, O. Boncalo, "Low-precision DSP-based floating-point multiply-add fused for Field Programmable Gate Arrays" IET Computing and Digital Techniques, Vol. 8, Issue 4, 2014
10. A.Amaricai, O.Boncalo, "Implementation of very high radix division in FPGAs" IET Electronic Letters, Vol. 48, Issue 18, 2012

For a complete list of publications, see:
https://scholar.google.com/citations?user=SnzPEh0AAAAJ&hl=en

Research Visits

June-July 2012 – University College Cork, Ireland, host: Lecturer Emanuel Popovici
January – February 2016, ENSEA, Cergy-Pontoise, France, host: Prof. David Declercq
August – December 2017 – Senior Fulbright Scholar – University of Arizona, Tucson, AZ, USA, host: prof. Bane Vasic; Research topic: Logarithmic Version for Generalized Belief Propagation (GBP)